UNC CHARLOTTE
The WILLIAM STATES LEE COLLEGE *of* ENGINEERING

Senior Design Project Description

Company Name	Internal ECE Dept	Date Submitted	April 01, 2020
Project Title	FPGA Secure Design Flow - Phase 2 **(UNCC_FLOW2)**	Planned Semester	Fall 2020 Spring 2021

Personnel:

Typical teams will have 4-6 students, with engineering disciplines assigned based on the anticipated Scope of the Project. 250 hours are expected per person.
Complete the following table if this information is known, otherwise the Senior Design Committee will develop based on the project scope:

Discipline	Number	Discipline	Number
Mechanical	0	Electrical	2
Computer	3	Systems	0
Other			

Project Overview:

Hardware security has become a major concern for electronic devices with outsourced semiconductor business model and integration of third party Intellectual property (3PIPs). Electronic devices are vulnerable to attacks such cloned attacks, reverse engineering, IP theft and over production during design process and fabrication, and to invasive and non-invasive during runtime. Field programmable gate arrays (FPGAs) are reconfigurable in nature and are inherently more secure since the design is loaded post manufacture. FPGA security relies on bitstream protection. In this project we will evaluate FPGA security and integrate security solutions and secure framework.

FPGAs IP are distributed in form of RTL, Netlists that can be reverse engineering and can be cloned or reused. This project will enable IPs to be modified in an automated manner for making the design resilient to reverse engineering using logic locking technique and webserver based secure key management framework.

Initial Project Requirements:

The students will work with Xilinx Zynq ZedBoards and Xilinx Pynq boards. Both boards are available in my research lab. The students will be given system, to install tools and will be able to use the space available in my research lab to conduct their research. Also, students will able to use the lab servers and computers for development and simulation.

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Expected Deliverables/Results:

The students will deliver an automated design flow, with integrated logic locking feature. The key management will be done on a webserver, where the connections between Webserver and the client node (FPGA device) programmed with locked IP will use TLS encryption. The students will submit the simulations and hardware demonstration of the SoC with integrated secure design flow.

Disposition of Deliverables at the End of the Project:

An automated secure design flow will be demonstrated on Xilinx Zynq boards.

List here any specific skills, requirements, knowledge needed or suggested (If none please state none):

Basic knowledge of computer organization and Introduction to VHDL is a MUST, and architecture is preferred. The students encourage to take the courses on computer organization (ECGR 3183), Introduction to VHDL (ECGR 4161) computer architecture course (ECGR 4181). Also, the basic understanding of C/C++ programming, python, embedded systems, Linux operating systems will be required.